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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|-----------------------|
| 09/890,226 | 06/07/2002 | Yves Reignoux | 09669/005001 | 7556 |
| 22511 | 7590 | 07/28/2004 | EXAMINER | |
| OSHA & MAY L.L.P. 1221 MCKINNEY STREET HOUSTON, TX 77010 | | | | GEBREMARIAM, SAMUEL A |
| | | ART UNIT | | PAPER NUMBER |
| | | 2811 | | |

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|----------------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 09/890,226 | REIGNOUX ET AL. | |
| | Examiner Samuel A Gebremariam | Art Unit 2811 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 06 May 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-7 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dehaine et al. US patent No. 4,774,633.

Regarding claim 1, Dehaine teaches (fig. 1) an integrated circuit device, characterized in that it comprises: an active chip (12) of a semiconductor material comprising an electrical circuit, the active chip having an active face (12a) provided with a plurality of electrical connection terminals (14) and a second face (12b), and a complementary chip (11) having a first face (opposite of 11a) attached to the active face of the active chip (attached through region 21), a second face (11a) and a side surface (side surface of 11), wherein the complementary chip has a plurality of recesses (regions between 11 wherein the connection terminals exist), each recess extending through the whole thickness of the complementary chip and extending from above a contact terminal to the side surface.

Dehaine does not explicitly teach the complementary chip has a larger thickness than the active chip wherein the active chip has a thickness of less than 100 um.

Parameters such as thickness and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust thickness of the active chip and complimentary chip as claimed in order to provide better protection.

Regarding claims 2 and 3, Dehaine teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the thickness of the active layer ranges from 5 to 50 μm and the thickness of the complementary layer ranges from 100 to 200 μm .

Parameters such as thickness and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the active chip and complementary chip in the structure of Dehaine within the range as claimed in order to form an integrated circuit card that is compactly packaged.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dehaine in view of Tada US patent No. 5,155,068.

Regarding claim 4, Dehaine teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the complementary chip is formed with the same semiconductor material as the active chip.

Tada teaches forming an LSI chip (40) and forming complementary chip (4a) on the active chip (4b) made of silicon.

LSI chips are routinely formed on silicon substrate it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same material to form both the complimentary chip and active chip as claimed in the structure of Dehaine since silicon is widely used in the fabrication of integrated circuits.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dehaine in view admitted prior art.

Regarding claim 5, Dehaine teaches substantially the entire claimed structure of claim 1 above except explicitly stating an insulating substrate having an outer face provided with outer electrical contact pads and an inner face, the second face of the active chip being attached to the substrate inner face.

Admitted prior art teaches (fig. 1) an insulating substrate (18) having an outer face provided with outer electrical contact pads and an inner face (upper surface of 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the insulating substrate taught by admitted prior art in the structure of Dehaine in order to provide a better support to the integrated circuit structure.

Furthermore the combined structure of Dehaine and admitted prior art would inherently have the second face of the active chip being attached to the substrate inner face, and a plurality of electrical leads, each lead having a first end connected to a contact terminal and a second end connected to an outer contact pad and lying entirely

between the plane containing the second face of the complementary chip and the insulating substrate (fig. 1 of admitted prior art).

Regarding claim 6, Dehaine teaches (fig. 1, admitted prior art) substantially the entire claimed structure of claim 1 above including the insulating substrate includes windows (26), each window being disposed above an outer electric contact pad (where lead 24 is connected).

Regarding claim 7, Dehaine teaches (fig. 1, admitted prior art) substantially the entire claimed structure of claim 1 above including an electronic unit according to claim 5.

Response to Arguments

5. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-E are cited as being related to smart card. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
July 25, 2004



EDDIE LEE
SUPERVISORY PATENT EXAMINER
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